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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,330	02/18/2004	Hideki Hirayama	35901-079001	9450

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EXAMINER	
ALUNKAL, THOMAS D	

ART UNIT	PAPER NUMBER
2627	

NOTIFICATION DATE	DELIVERY MODE
08/14/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

INFO@ORTPATENT.COM

Office Action Summary	Application No.	Applicant(s)	
	10/781,330	HIRAYAMA ET AL.	
	Examiner	Art Unit	
	THOMAS D. ALUNKAL	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-7,10 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-7,10 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

hiContinued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/21/08 has been entered.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-7, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino et al. (hereafter Minamino)(US 6,657,929) and in view of Katoh (US 6,088,311) and Kubo et al. (hereafter Kubo)(US 5,563,860).

Regarding independent claim 10, Minamino discloses a clock generating device for generating a clock signal synchronizing with a wobble signal, which includes address information for a predetermined period (see Abstract and Figure 9), the clock device comprising: a PLL circuit for generating an oscillation signal in accordance with the difference between the phase of a wobble signal and the phase of a clock signal and for

generating the clock signal by synchronizing the oscillation signal with the wobble signal (Column 8, lines 45-47); and a detection circuit, connected to the PLL circuit, for monitoring the wobble signal, detecting the predetermined period of the wobble signal that includes the address information and holding the frequency of the oscillation signal of the PLL circuit in accordance with the detection (Column 8, lines 45-58); wherein the detection circuit includes: a hold signal generator for generating a first hold signal that holds the frequency of the oscillation signal of the PLL circuit during a first period in accordance with the detection (Figure 10, Element 72 and Column 17, lines 10-37), a second hold circuit (Figure 10, Element 73), and a signal selector connected to the hold signal generator (Column 17, lines 38-42), wherein the PLL circuit includes: a phase comparator circuit for generating a phase difference signal in accordance with the difference between the phase of the wobble signal and the phase of the oscillation signal (Column 1, lines 25-29 and Column 8, lines 50-53). Minamino does not specifically disclose wherein the second wobble failure detection circuit 73 is used for generating a hold signal. Rather, Minamino discloses that the signal exiting the second wobble failure detection circuit 73 (which has the same properties as the signal exiting first wobble failure detection circuit 72, expect for the time period each is based on (t1 and t2)) is inverted into a wobble usable signal.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to omit the inverter disclosed in Figure 10 of Minamino to produce two separate hold signals to be selectively input to the wobble PLL circuit, since it has been held that the omission of an element and its function in a combination

where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson*, 136 USPQ 184.

In addition, Minamino does not disclose but Katoh does disclose a charge pump, connected to the phase comparator, for generating an output signal in accordance with the phase comparator and the charge pump stops functioning in response to one of the first hold signal and the second hold signal (Column 14, lines 6-31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to supplement the teachings of Minamino and have a charge pump, connected to the phase comparator, for generating an output signal in accordance with the phase comparator and the charge pump stops functioning in response to one of the first hold signal and the second hold signal, as disclosed by Katoh, motivation being to control the gain of the PLL circuit according to the frequency of the input data.

Furthermore, Minamino does not disclose wherein the clock generating device further comprises a frequency divider connected to the phase comparator, for generating a divisional signal by dividing the oscillation signal by a predetermined dividing ratio, and providing the divisional signal to the phase comparator so that the phase comparator generates a phase difference signal in accordance with the difference between the phase of the wobble signal and the phase of the divisional signal, wherein the frequency divider changes the dividing ratio in accordance with the cycle of the wobble signal. In the same field of endeavor, Kubo discloses a clock generating device comprising a PLL (Figure 2, Element 25), which includes a frequency

divider providing a divisional signal to a phase comparator, and the dividing ratio of the frequency divider is variable in accordance with the cycle of a wobble signal (Figure 2, Element 28, Column 3, lines 31-46, and Column 4, lines 3-12).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to supplement the teachings of Minamino, and have a frequency divider, connected to the phase comparator, for generating a divisional signal by dividing the oscillation signal by a predetermined dividing ratio, and providing the divisional signal to the phase comparator so that the phase comparator generates a phase difference signal in accordance with the difference between the phase of the wobble signal and the phase of the divisional signal, and the frequency divider changes the dividing ratio being changed in accordance with the cycle of the wobble signal, motivation being to stabilize the loop gain of the PLL channel.

Regarding claim 3, Minamino discloses wherein the first period is shorter than the predetermined period, and the second period is longer than the predetermined period (hold signal is kept at low level before the clock count exceeds t1 and at a high level when it exceeds t1, Column 17, lines 10-37).

Regarding claim 4, Minamino discloses wherein the cycle of the wobble signal changes with at least two timings in accordance with the address information of the predetermined period, and the hold signal generator generates a first hold signal for holding the frequency of the oscillation signal of the PLL circuit during a period between a first timing and a second timing, at which the cycle of the wobble signal changes (Column 17, lines 38-42).

Regarding claim 5, Minamino discloses wherein the cycle of the wobble signal changes during the predetermined period, and the hold signal generator generates the second hold signal for holding the frequency of the oscillation signal of the PLL circuit during the second period, which is longer than the first period of the first hold signal, from a timing at which the cycle of the wobble signal changes (Column 17, lines 10-37).

Regarding claim 6, Minamino discloses a synchronization protection circuit, connected to the detection circuit, for performing counting in accordance with the wobble signal, estimating the predetermined period during which the address information is included in the wobble signal, and generating a synchronization protection signal in accordance with the estimated period, the signal selector of the detection circuit providing the PLL circuit with one of the first hold signal, the second hold signal, and the synchronization protection signal (Column 4, line 66-Column 5, line 20).

Regarding claim 7, Katoh discloses wherein at least one of the phase comparator and the charge pump stops functioning in response to one of the first hold signal, the second hold signal, and the synchronization protection signal (Column 14, lines 6-31).

Regarding independent claim 13, Minamino discloses a clock generating device for generating a clock signal synchronizing with a wobble signal that includes address information during a predetermined period, wherein the cycle of the wobble signal changes with at least two timings in accordance with the address information of the predetermined period (see Abstract and Figure 9), the clock generating device comprising: a PLL circuit for generating an oscillation signal in accordance with the difference between the phase of the wobble signal and the phase of the clock signal

and for generating the clock signal by synchronizing the oscillation signal with the wobble signal (Column 8, lines 45-57); a monitor, connected to the PLL circuit for monitoring the wobble signal, wherein the monitor generates a first hold signal (Figure 10, Element 72 and Column 17, lines 10-37) that holds the frequency of the oscillation signal of the PLL circuit during a first period between a first timing and a second timing, at which the cycle of the wobble signal changes, and a second hold signal (Figure 10, Element 73) that holds the frequency of the oscillation signal of the PLL circuit during a second period, which is longer than the first period of the first hold signal measured from the first timing (Column 17, lines 10-37); a signal selector, connected to the monitor (Column 4, line 66-Column 5, line 20); and a synchronization protection circuit for performing counting in accordance with the wobble signal, estimating the predetermined period during which the address information is included in the wobble signal, and generating a synchronization protection signal in accordance with the estimated period, the signal selector of the detection circuit providing the PLL circuit with one of the first hold signal, the second signal, and the synchronization protection signal (Column 4, line 66-Column 5, line 20), wherein the PLL circuit includes: a phase comparator circuit for generating a phase difference signal in accordance with the difference between the phase of the wobble signal and the phase of the oscillation signal (Column 1, lines 25-29 and Column 8, lines 50-53). Minamino does not disclose wherein the second wobble failure detection circuit 73 is used for generating a hold signal. Rather, Minamino discloses that the signal exiting the second wobble failure detection circuit 73 (which has the same properties as the signal exiting first wobble

failure detection circuit 72, expect for the time period each is based on (t1 and t2)) is inverted into a wobble usable signal.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to omit the inverter disclosed in Figure 10 of Minamino to produce two separate hold signals to be selectively input to the wobble PLL circuit, since it has been held that the omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson*, 136 USPQ 184.

In addition, Minamino does not disclose but Katoh does disclose a charge pump, connected to the phase comparator, for generating an output signal in accordance with the phase difference signal, wherein at least one of the phase comparator and the charge pump stops functioning in response to one of the first hold signal, the second hold signal, and the synchronization protection signal (Column 14, lines 6-31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to supplement the teachings of Minamino and have a charge pump, connected to the phase comparator, for generating an output signal in accordance with the phase comparator and the charge pump stops functioning in response to one of the first hold signal, the second hold signal, and the synchronization protection signal, as disclosed by Katoh, motivation being to control the gain of the PLL circuit according to the frequency of the input data.

Furthermore, Minamino does not disclose wherein the clock generating device further comprises a frequency divider connected to the phase comparator, for

generating a divisional signal by dividing the oscillation signal by a predetermined dividing ratio, and providing the divisional signal to the phase comparator so that the phase comparator generates a phase difference signal in accordance with the difference between the phase of the wobble signal and the phase of the divisional signal, wherein the frequency divider changes the dividing ratio in accordance with the cycle of the wobble signal. In the same field of endeavor, Kubo discloses a clock generating device comprising a PLL (Figure 2, Element 25), which includes a frequency divider providing a divisional signal to a phase comparator, and the dividing ratio of the frequency divider is variable in accordance with the cycle of a wobble signal (Figure 2, Element 28, Column 3, lines 31-46, and Column 4, lines 3-12).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to supplement the teachings of Minamino, and have a frequency divider, connected to the phase comparator, for generating a divisional signal by dividing the oscillation signal by a predetermined dividing ratio, and providing the divisional signal to the phase comparator so that the phase comparator generates a phase difference signal in accordance with the difference between the phase of the wobble signal and the phase of the divisional signal, and the frequency divider changes the dividing ratio being changed in accordance with the cycle of the wobble signal, motivation being to stabilize the loop gain of the PLL channel.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Konishi (US 6,104,682) discloses a disk apparatus having a data

reproducing system using a digital PLL. Maekawa (US 6,606,286) discloses a track loss signal generating apparatus used in an optical disc drive equipped with amplitude adjusting apparatus for a tracking error signal. Tanoue et al. (US 5,469,417) discloses an information recording/reproducing apparatus for recording or reproducing data, and clock generating circuit incorporated therein. Morishima (US PgPub 2003/0198152) discloses a method of consecutive writing on recording discs. Liaw (US 6,961,293) discloses a method and related device for achieving stable writing state of compact disk drive by adjusting writing clock. Takeuchi et al. (US 5,528,574) discloses a disk reproducing apparatus capable of increasing speed of access to disks recorded at a constant linear velocity.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THOMAS D. ALUNKAL whose telephone number is (571)270-1127. The examiner can normally be reached on M-F 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on (571)272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the

Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TAN Xuan DINH/
Primary Examiner, Art Unit 2627
August 11, 2008

/Thomas D Alunkal/
Examiner, Art Unit 2627